unpatentable over U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully traverses the rejections, and requests reconsideration and reexamination of all rejected claims 1-20.

Summary of Invention

The present invention provides a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Rejection of claims 15-20 under 35 U.S.C. § 101

The Office Action rejected claims 15-20 under 35 U.S.C. § 101 because "the claimed computer program ... is not transformed into a useful product carrying a practical application as stated in 101 title." Curiously, the previous Office Action rejected only claim 15 under 35 U.S.C. § 101. The present Office Action, however, rejects claims 15-20, and Applicant does not understand why the treatment differs. Nevertheless, Applicant traverses this rejection for the reasons set forth below.

As Applicant noted in his prior response, claims 15-20 were amended to change the focus of the claims from being directed to a computer program to instead direct the claims to a computer readable medium. The present Office Action, however, mischaracterizes these claims as being directed to a computer program. Further, the present Office Action erroneously states that the claims "are not a statutory subject matter because [the computer program] is not transformed into a useful product..." Applicant respectfully disagrees.

First, the "transformation" language recited by the Office Action is not relevant to the claims at hand. Instead, this language is pertinent only when addressing method claims that effectively define a mathematical algorithm. In this regard, the Patent Office has taken the position that claims otherwise directed to mathematical algorithms must set forth (within the claims) a practical application in order to qualify as statutory subject matter.

Claims 15-20 of the present application, however, are not method claims and cannot therefore be treated as mathematical algorithms. Instead, the claims are directed to a computer readable medium, which is clearly statutory subject matter. The fact that the claims recite program code as a part of the computer readable medium does not change this analysis. Computer-readable media are legitimate statutory subject matter for patents. Therefore, the rejection of claims 15-20 should be withdrawn.

Fundamental Distinction of the Ikeda Patents

Applicant respectfully traverses the rejections of claim 1-20 of the present application based upon Ikeda, for reasons that will be specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Ikeda and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. The Ikeda patent only mentions the term "noise" in the context of crosstalk noise, and not in the manner taught and treated by the present invention.

In this regard, Ikeda recognizes that a transistor having low output impedance is prone to exert the influence of crosstalk on other wires. However, Ideka also recognizes that a transistor of high output impedance is susceptible to crosstalk from other wires. Accordingly, the system of the Ikeda patent is concerned with crosstalk verification. Furthermore, the system disclosed by Ikeda appears to reference wire patterns and the capacitance measurements therebetween to determine whether crosstalk noise will be problematic.

Discussion of Specific Rejections based upon Ikeda

Turning now to the specific rejections, the Office Action rejected claims 1-20 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully traverses this rejection for at least the reasons that follow.

In rejecting claims 1 and 15, the Office Action states only:

> As per claims 1 and 15, Ikeda anticipated method and operation system for checking design rule as claimed. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters

such as width, length, connected in device channel, etc. (see cols. 2-7). The program is designed to check noise susceptible in the circuit (col. 2, lines 7-24), including checking noise immunity as claimed because they are parts of noise control scheme.

This was the complete rejection set forth for claims 1 and 15.

First, Applicant submits that the general reference to "cols. 2-7" is too general and vague to comply with the requirements of MPEP 707.07 *et seq.*, which requires that all rejections be stated with completeness and clarity. More specifically, MPEP § 707.07(d) requires that the grounds for rejection be "fully and clearly stated." For this reason alone, the rejections should be withdrawn.

As a further example of the Office Action's failure to adequately reject the claims, the rejection of claim 2 merely states:

> As per claim 2, Ikeda anticipated reading transistor design parameters for design rule check as claimed.

However, claim 2 recites:

> 2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Clearly, the rejection fails to point to the teachings within Ikeda that allegedly disclose the claimed features of claim 2. Similar deficiencies exist in the other claim rejections as well. Therefore, these rejection should be withdrawn for these reasons. Should an ensuing Office Action be mailed, which provides more detail in this regard, such an ensuing Office Action must be made non-Final.

Claims 1-7

Notwithstanding the only generalized rejection advanced by the Office Action, the undersigned has closely reviewed the Ikeda reference and submits that it does not disclose the invention as defined by the independent claims of the present application. Turning first to independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
>
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 1 for at least the reason that Ikeda fails to disclose or teach at least the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of crosstalk noise as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract). In contrast, claim 1 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate has an acceptable noise immunity. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 1 is misplaced and should be withdrawn. For at least these same reasons, claims 2-7, which depend from claim 1, patently define over Ikeda as well.

Claims 8-14

The Office Action also rejected claims 8-14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and
>
> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Ikeda fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8 stating only:

> As per claim 8, Ikeda anticipated the method for checking design rule including checking transistor design parameters in compatible with different operating conditions or with different transistor layout configuration such that susceptible noise would be checked for high power voltage, heat generation, different transistor threshold, etc., 'Background of the Invention', col. 2, lines 7-24.

The cited portion (col. 2, lines 7-24) of Ikeda specifically recites:

> In the crosstalk verification device, the first extracting means extracts from the layout pattern data the output wiring patterns of the transistor prone to exert crosstalk influence and the transistor susceptible to crosstalk. Then the second extracting means determines the wire-to-wire capacitance of the overlap/parallel portion between the output wiring patterns of the two transistors to calculate the magnitude of crosstalk noise produced when the output signal of the transistor susceptible to crosstalk rises and falls as a function of the wire-to-wire capacitance. The calculated magnitude of crosstalk noise, if exceeding the third reference, is extracted as the error portion. The display means visually displays the error portion. This affords the automatic verification of the crosstalk. The correct crosstalk

verification is enabled when the scale of the integrated circuit is expanded or reduced.

As can be readily verified from even a cursory review of the cited portion of Ikeda, this cited portion does not disclose a step of "***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity,***" which is specifically claimed in claim 8.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 8 is misplaced and should be withdrawn. For at least these same reasons, claims 9-14, which depend from claim 8, patently define over Ikeda as well.

Claims 15-20

The Office Action also rejected claims 15-20 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 5,446,674 to Ikeda. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 15 recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 15 for at least the reason that Ikeda fails to disclose or teach either of the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of crosstalk noise as a function of the wire-to-wire capacitance, in

order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract). In contrast, claim 15 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate has an acceptable noise immunity. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 15 is misplaced and should be withdrawn. For at least these same reasons, claims 16-20, which depend from claim 15, patently define over Ikeda as well.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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